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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,450	04/19/2001	Satoshi Ishikura	60188-051	6764

7590 06/19/2003

MCDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER
OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,450	ISHIKURA ET AL.	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *8-13* is/are allowed.

6)☒ Claim(s) *1-4,7 and 14-17* is/are rejected.

7)☒ Claim(s) *5,6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1, 2, 3, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by US patent No. 5,998,843 to Yoshida.

Regarding claim 1, Yoshida teaches a semiconductor device (Fig. 10, for example), comprising:

a source/drain (19) layer for a transistor; and

a dummy diffused layer (7);

wherein, the source/drain layer has its surface silicided (26), and

wherein the dummy diffused layer has its surface covered with an anti-silicidation film (5), on which no gate electrode is provided.

Regarding claim 2, Yoshida teaches a semiconductor device, wherein the anti-silicidation film is an oxide film (Col. 4, lines 63 – 64).

Regarding claim 3, Yoshida teaches a semiconductor device, wherein a dopant, which has been introduced into the source/drain layer has not been introduced into the dummy diffused layer (different dopant types).

Regarding claim 14, Yoshida teaches a semiconductor device comprising:

a source/drain (19) layer for a transistor; and

a dummy diffused layer (7);

wherein, the source/drain layer has its surface silicided (26), and

wherein the dummy diffused layer has its surface covered with an anti-silicidation film (5), and

wherein the dummy diffused layer is located between an analog circuit block and a digital circuit block.

Regarding claim 15, Yoshida teaches a semiconductor device, comprising:

a source/drain (19) layer for a transistor; and

a dummy diffused layer (7);

wherein, the source/drain layer has its surface silicided (26), and

wherein the dummy diffused layer has its surface covered with an anti-silicidation film (5), and

wherein, the dummy diffused layer is not electrically coupled to another component via an interconnect.

3. Claims 4, 7, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent No. 6,455,894 to Matsumoto et al.

Regarding claim 4, Matsumoto et al. teaches a semiconductor device (Fig. 9), comprising:

a substrate (1);

a source/drain diffused layer (6b, 6a) formed in the substrate for a transistor; and

a dummy diffused layer (6d, 6c) formed in the substrate;

wherein the source/drain diffused layer has its surface silicided (10b,10a), and

wherein, the dummy diffused layer has its surface partially covered with a dummy gate electrode (7c).

Regarding claim 7, Matsumoto et al. teaches a semiconductor device, wherein a dopant, which has been introduced into the source/drain diffused layer, has not been introduced into the dummy diffused layer (different dopant type).

Regarding claim 16, Matsumoto et al. teaches a device, wherein the dummy diffused layer is located between a circuit block (TR1) and another circuit block (DM3, TR1).

Regarding claim 17, Matsumoto et al. teaches a device, wherein the dummy diffused layer is not electrically coupled to another component via an interconnect.

Allowable Subject Matter

4. Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 8 – 13 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach a gate electrode divided into portions, nor the dummy gate being held at a fixed potential.

Response to Arguments

7. Applicant's arguments with respect to claims 1 – 4, 7 and 14 – 17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DWO
June 13, 2003